

# Xilinx XQRKU060 Update for XRTC

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# Next Generation Space (XQR) Kintex® UltraScale™ Product



## > Kintex UltraScale First 20nm FPGA for Space Applications

- >> Deploys same commercial silicon mask set
- >> Utilizes Vivado Ultrafast Development Advantage



## > Kintex UltraScale in Ruggedized Ceramic Column Grid Array (CCGA)

- >> 40mm x 40mm package
- >> Footprint compatible with commercial A1517 package



## > Product Space Test Flows

- >> B-Flow (QML-Q Equivalent) & Y-Flow (QML-Y Compliant)
  - Per MIL-PRF-38535 Revision K for ceramic non-hermetic packages in space applications, designated as Class Y

# XQRKU060-CNA1509 Product Overview

Resource		XQRKU060
Logic Resources	System Logic Cells (K)	726
	CLB Flip-Flops	663,360
	CLB LUTs	331,680
Memory Resources	Maximum Distributed RAM (Kb)	9,180
	Block RAM/FIFO w/ECC (36Kb each)	1,080
	Block RAM/FIFO (18Kb each)	2,160
	Total Block RAM (Mb)	38
	Maximum Distributed RAM (Kb)	9,180
	Block RAM/FIFO w/ECC (36Kb each)	1,080
Clock Resources	Maximum Single-Ended HP I/Os	520
	Maximum Differential HP I/O Pairs	240
	Maximum Single-Ended HR I/Os	104
	Maximum Differential HR I/O Pairs	48
Integrated IP resources	DSP Slices	2,760
	System Monitor	1
	PCIe <sup>®</sup> Gen1/2/3	3
	Interlaken	0
	100G Ethernet	0
	12.5Gb/s Transceivers (GTH)	32*
Military (-55°C to +125°C)		-1 (Speed Grade)
Package Footprint		Package Dimensions (mm)
Commercial Prototype Vehicale A1517		40x40
Flight Pacakage CNA1509		40x40
		HR I/O, HP I/O, GTH
		104, 520, 32
		104, 516, 32

Product Table

Supports 32 GTHs!

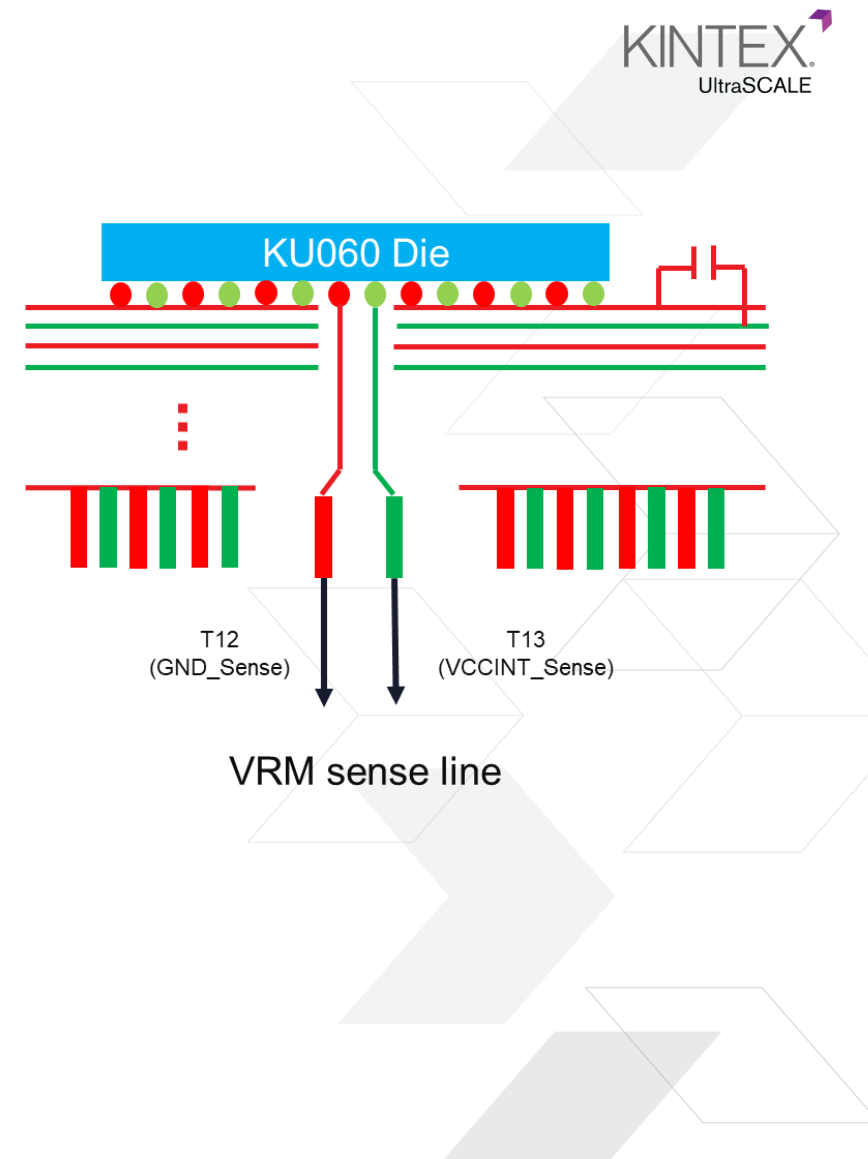
\*Note : Designers can use the 32<sup>nd</sup> RX pair mapped from AV1/AV2 → T1/T2

# CNA1509 Package Characteristics

- > **XQR KU060 CNA1509 ceramic package for space applications is based on the existing XC KU060 A1517 organic package to ensure footprint compatibility**
  
- > **CNA1509 Package characteristics**
  - >> 40mm x 40mm ceramic design
  - >> Utilizes 2.2mm long column grid array (CGA) columns - Sn/Pb and Cu ribbon
  - >> Pinout for CNA1509 modified from FFVA1517
    - Corner pins removed for handling & vibration considerations
  - >> Utilizes package decoupling capacitors rated to 125° C and qualified for XQ applications
  - >> Due to higher resistivity of Ceramic material specific package optimizations were implemented

# CNA1509 Package Optimizations

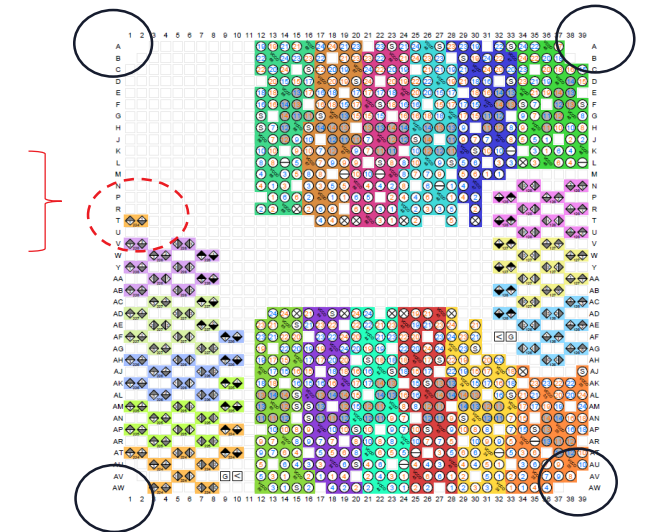
1. Added a pair of dedicated VCCINT/GND pins for sensing at C4 bumps
2. Raised Nominal Voltage for all power rails
3. Merged VCCINT/VCCINT\_IO Rails on the package
  - Xilinx currently recommends tying these rails on the PCB



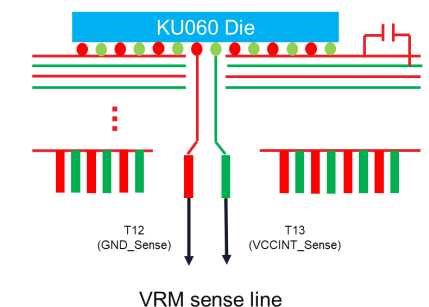
# XC to XQR Migration Guideline

- XQRKU060 CNA1509 ceramic package pinout is footprint compatible with XCKU060 A1517 package
- Supports 32\* GTHs

Bank/Quad	Pin	Commercial Package 1517 Function	Space grade Package 1509 Function
Quad 224	AV1	MGTHRXN1,	Absent ( function Relocated to T1*)
Quad 224	AV2	MGTHRXP1	No Connect (since AV1 removed- function relocated to T2*)
Bank 25	AV39	IO_L8N (diff pair with AV3 8)	Absent
Bank 25	AV38	IO_L8P (diff pair with AV39)	Single Ended IO
Bank 25	AW38	Single-ended IO	Absent
Bank 46	A38	(IO_L17N) (diff pair with A37)	Absent
Bank 46	A37	(IO_L17P), diff pair with A38)	Single Ended IO
Bank 46	B39	(IO_L16N), diff pair with C38	Absent
Bank 46	C38	(IO_L16P), diff pair with B39)	Single Ended IO
	AW2, A2, B1	GND, GND, NC	Absent
	T12, T13	VCCINT/GND PAIR	Sense Line ; T13 (VCCINT_SENSE), T12 (GND_SENSE)



CNA1509 Package – XCKU060 I/O Bank Diagram



\*Designers can use the 32<sup>nd</sup> RX pair mapped from AV1/AV2 → T1/T2

# CNA 1509 Package Optimization

## 2. Elevated the nominal voltage for all the Core, MGT, IO power rails

>> Operating voltages for some key power rails are shown below

Power Rail	XC 1517 Package Nominal Voltage (V)	XQR CNA1509 Package Nominal voltage (V)
VCCINT	0.95	1.01
VCCBRAM	0.95	1.01
VCCAUX	1.80	1.884
MGTAVCC	1.00	1.030
MGTAVTT	1.20	1.230
MGTVCCAUX	1.80	1.830
VCCO (HP IO)	1.0 – 1.8	1.884

- New spec meets lifetime reliability

# Board Design Considerations

- > **Choose a VRM with DC tolerance of +/- 2% or better to power the FPGA device**
  - >> Tolerance for AC noise included in timing analysis
- > **Ensure the VCCINT VRM sense line pins on the voltage regulator are connected to the dedicated pair of VCCINT/GND ball pair identified for sense line connection**
- > **Make sure the VCCINT VRM is sized appropriately to handle current from VCCINT, VCCINT\_IO since they are tied together on the package**
- > **Ensure adequate PCB decoupling on power rails to minimize the low frequency noise**





# XQRKU060-CNA1509 Schedule

## > Early programs may proceed directly to development

- >> Commercial Device : Pin compatible commercial XCKU060/A1517 device available now!
- >> Software : Target XCKU060/A1517 (-1 Speed Grade) in Vivado software
- >> Platforms for Prototyping
  - [Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit](#) (XCKU040-2FFVA1156E) available now!
  - Kintex UltraScale Space development kit (from Alpha Data) available **NOW!**
    - Will be possible to mount either XC or XQR part on Space Development board

## > Flight Part Schedule

- >> November 2018 – Package Design Released / Pin Map Available
- >> March 2019 – Package Substrate Manufacturing Complete
- >> June 2019 – Package Assembly Complete
- >> December 2019 – Pre-qualification Complete
- >> September 2020 – “Y” Availability XQRKU060-CNA1509Y

**Thank You**

**Adaptable.**  
**Intelligent.**

